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RESEARCH ARTICLE

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Improvement of Read Performance Using CMOS on Array (COA) in 3D NAND Flash

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Abstract: 2D NAND flash cells were unable to continue scaling due to several physical limitations including few electron effects, cell-to-cell interference, and high E-fields under 20 nm design rule. 3D NAND flash cell was developed to overcome many problems for 2D NAND cell. Also, it has continued to deliver and even accelerate the NAND scaling trends that the data industry demands. This is in part due to its larger gate area and improved electrostatics of the Gate All Around architecture using the thin poly-silicon channel. It has not only improved the cell characteristics such subthreshold swing and current but also reduced cell interference. As a result, the 3D NAND flash with superior performance has been currently enabled for three and four bit per cell to become main stream. 3D NAND architectures adapted "poly-Si channels," "word line replacement for metallization," and "plug etching process." In addition, to overcome the issue of peripherals taking up too large an area and too high a percentage of the total die size, a few different architectures were proposed. The peripheral circuit (CMOS) can be under array and another alternative is to build the peripheral circuits on a different CMOS wafer and then bond the memory wafer with the CMOS wafer using wafer-to-wafer microbonding, termed CMOS bonded array. Although the two architectures have many advantages for NAND cell, they still are suffering the degradation of read performance due increased BL RC delay. As NAND stack increases, it should be more challenge due to higher stack. In this paper, the new structure was proposed using NC-vTFT (NAND Cell-vertical TFT) on cell array in vertical NAND flash memory, for the first time. It will be very promising structure to improve RC delay as NAND cell stack increases.

Keywords: 3D NAND flash, NC-vTFT, COA structure, RC delay

1. Introduction

NAND flash memory is one of the most important nonvolatile memory devices that can hold programmed data without a power supply. With the wide spread of the portable equipment in audio/video fields such as MP3 players, digital cameras, and still mobile phone, the demand for low-cost and high-density flash memory has increased dramatically. NAND FLASH memory has dramatically increased density and reduced cost per bit which has driven creation of exciting new storage products over the years. These applications commonly need solid-state mass storage devices that feature high-density, low-cost, low power, nonvolatile, and portability. 2D NAND flash memory can easily satisfy the above needs. However, 2D NAND flash cells were unable to continue scaling due to several physical limitations including few electron effects, cell-to-cell interference, and high E-fields under 20 nm design rule. 3D NAND flash cell was developed to overcome many problems for 2D NAND cell. Recently, various 3D NAND flash memories such as stacked memory array transistor [1, 2], P-BiCS [3–5], TCAT [6, 7], V-NAND with Selective Epitaxial Gate (SEG) [8–11], and vertical gate [12, 13], which consists of the thin film poly-silicon (poly-Si) channel [14–17], have been introduced to be the most promising near-term solution to overcome scaling challenges in conventional planar NAND flash memories [18–23]. However, the side array and peripheral circuits in 3D NAND memory are like a ranch house in a crowded metropolitan downtown, where land is very precious. As the memory buildings grow taller, the peripheral circuits take a higher percentage of the total die size. As a result, 3D NAND scaling cost benefits are reduced accordingly [24, 25]. To find out the solutions for the issue of peripherals taking up too large an area and too high a percentage of the total die

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Figure 1
(a) Existing CUA structure, (b) proposed COA structure to improve BL RC delay, (c) bit line (BL) sensing schematic for CUA and COA

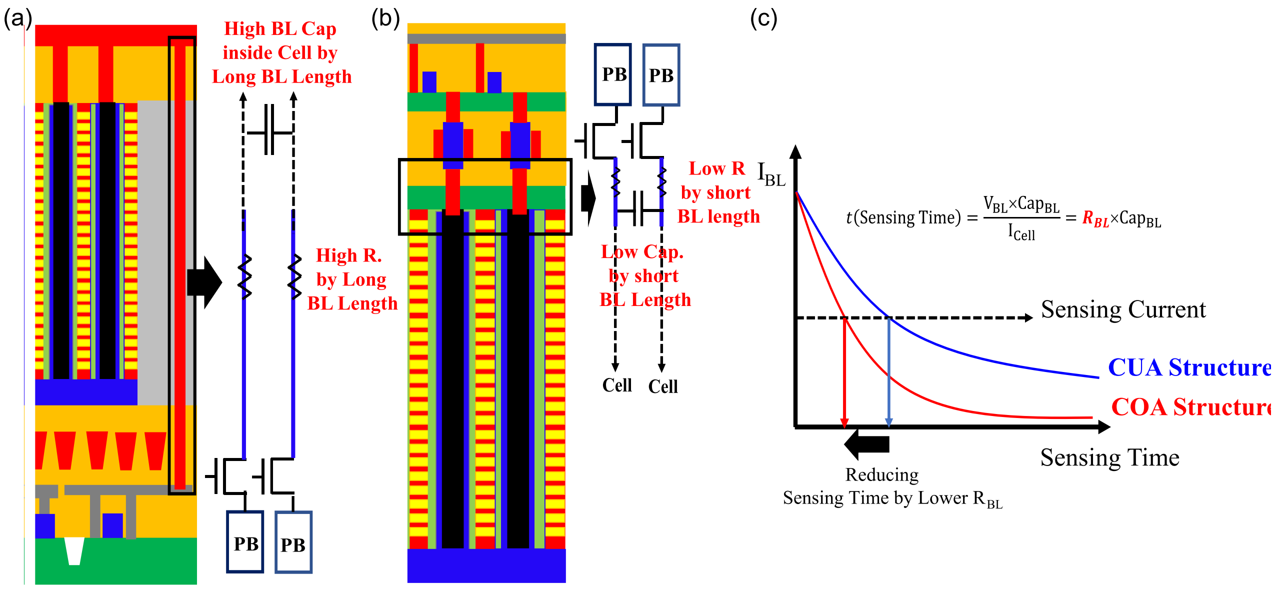
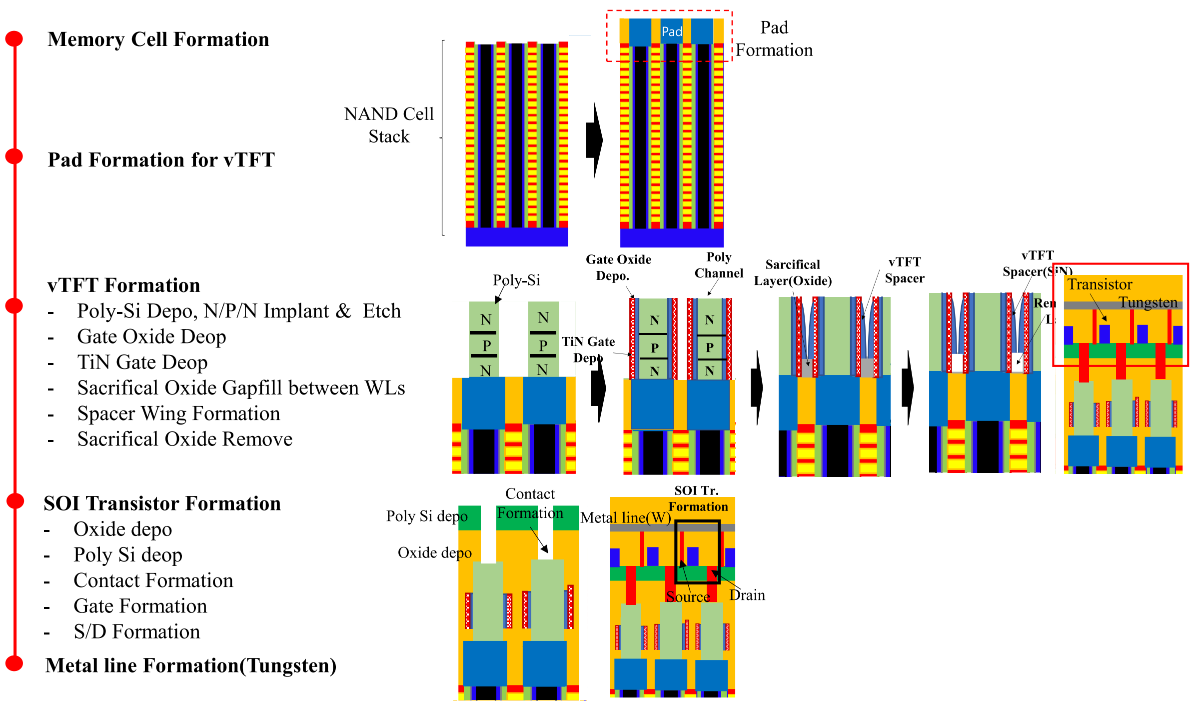


Figure 2
Process flow schematic for proposed COA structure



size, few different architectures were explored. As shown in Figure 1(a), the peripheral circuit (CMOS) can be under array (CUA). Another alternative is to build the peripheral circuits on a different CMOS wafer and then bond the memory wafer with the CMOS wafer using wafer-to wafer microbonding, termed as CMOS bonded array (CBA) [26, 27] to improve the performance of CMOS transistors. Although both architectures have many advantages for NAND flash cell, they still are suffering from the degradation of read performance by increased BL RC delay as shown in Figure 1(a). As the height of 3D NAND flash stack recently increases by 232 layers, it should be more challenging due to higher stack [28–30]. In this paper, we proposed new NAND flash cell structure using the vertical TFT (NC-vTFT) to improve the read and program performance through using reduced Bit line RC delay.

2. Process Flow and Simulation

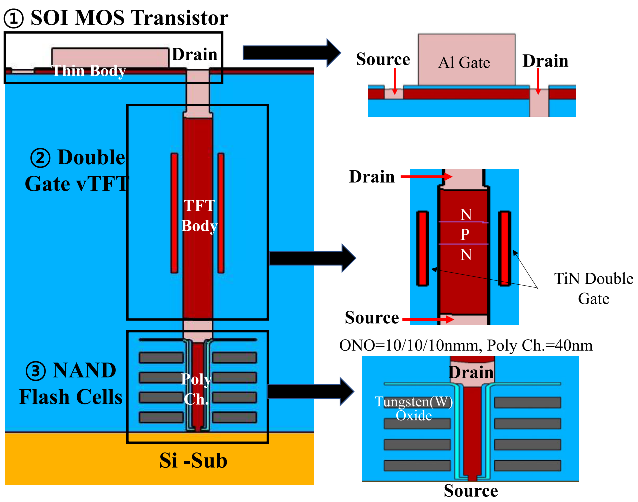
2.1. Process flow for structure

Figure 1(a) shows the CUA structure is suffered by RC delay of Equation (1) due to increased BL (Bit Line) length as the height of NAND stack recently increases. Compared to Figure 1(a), the proposed structure can improve the RC delay as shown in Figure 1(b) [28, 31, 32].

$$\mathrm{t} = \frac{\mathrm{V_{BL}} \times \mathrm{Cap_{BL}}}{\mathrm{I_{Cell}}} = \mathrm{R_{BL}} \times \mathrm{Cap_{BL}} \tag{1}$$

It is because that BL resistance would be largely decreased by shorter bit line length of CMOS structure on cell array (COA). It can be explained by Equation (1) as function of BL voltage (V_{BL}) and BL capacitance (Cap_{BL}) and NAND cell current ($\mathrm{I_{cell}}$) as shown in Figure 1(c). Figure 2 shows the process flow to fabricate the COA structure. Firstly, NAND flash cells are fabricated using existing 3D NAND flash process flow TCAT [6, 7], V-NAND with SEG [8–11], and vertical gate [12, 13], and vTFT(vertical Thin-Film-Transistor) is used for a high-voltage transistor to control the program and erase operations with vertical channel on NAND cell structure [33]. The air gap process was applied for vTFT as shown in Figure 2 [34]. After that CMOS transistors can be fabricated using SOI or Fin-FET transistor on vTFT. SOI transistor was introduced in this paper.

Figure 3
Simulation structure using the Athena process of Silvaco to fabricate the proposed structure. It is divided into 3 areas: ① SOI transistor, ② vTFT, and ③ NAND flash cells



2.2. Simulation for structure

Figure 3 shows the simulation structure that fabricated (1) SOI transistor, (2) vTFT, and (3) flash cell using Athena Silvaco TCAD Tool based on the process flow proposed in Figure 2. The detailed device parameters of simulation structure are listed in Table 1.

3. Results and Discussion

3.1. SOI transistor characteristics

Figure 4(a) and (b) show the secured I_d-V_g and I_d-V_d characteristics depending on channel boron doping and gate voltage for transistor with SOI, respectively. It was confirmed that they are normally operated. However, as the arsenic (As) implant energy increases for the drain doping, I_d abruptly decreases as shown in Figure 5(a). It is because of the higher drain resistance and less short channel effect in Figure 5(b) by deeper the arsenic doping profile in Figure 5(c).

Figure 4
(a) I_d-V_g curve depending on boron, (b) doping for CMOS transistor and I_d-V_d curve depending on gate voltage

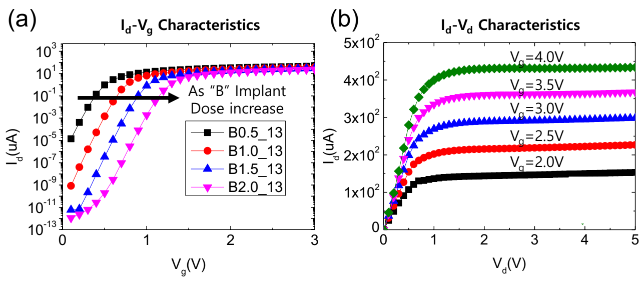


Table 1
Detailed Spec. for simulation

	Source/Channel/Drain Implant Dose and Energy	Gate or WL Length (um)	SOI /vTFT/Cell Poly Thickness (nm)
SOI Transistor	Source: As 1×10^{15}/cm^2, 10 KeV Channel: B 1E13, 10 KeV Drain: As 1.0E15, 10 KeV	0.4	Thin Body Thickness=20 Gate Oxide=7
vTFT	Source: Ph 4×10^{13}/cm^2, 1000 KeV Channel: B 1×10^{13}/cm^2 180 KeV Drain: Ph 1×10^{15}/cm^2 60 KeV	1.0	TFT Body Thickness=100 Gate Oxide=20
NAND Cell	Source: Doped Poly Ph 10^{21}/cm^3 Channel: Doped Poly B 4×10^{17}/cm^3 Drain: As 1E15, 50KeV	0.05 (Space=0.05)	Poly Ch. Thickness= 40 Oxide/Nitride/Oxide =10/10/10

Figure 5
(a) Linear scale and (b) log scale I_d-V_g curve depending on As implant energy, (c) doping profile depending on As implant energy

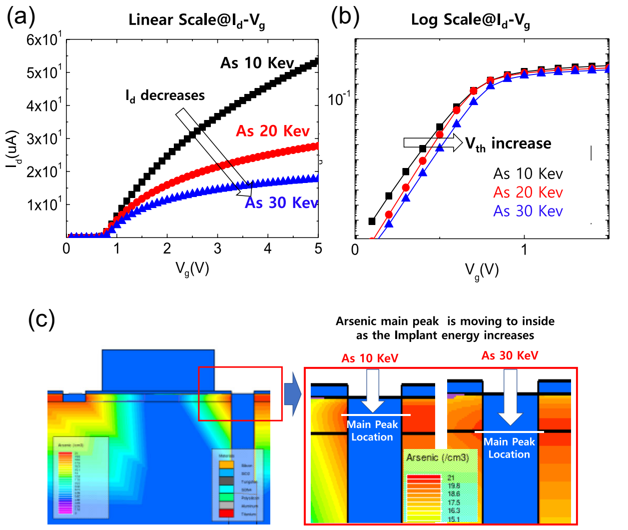


Figure 6
(a) Detailed process flow for proposed vTFT structure. (b) L_{eff} of vTFT for Ph implant energy depending on Ph implant dose. (c) Channel length depending on Ph energy

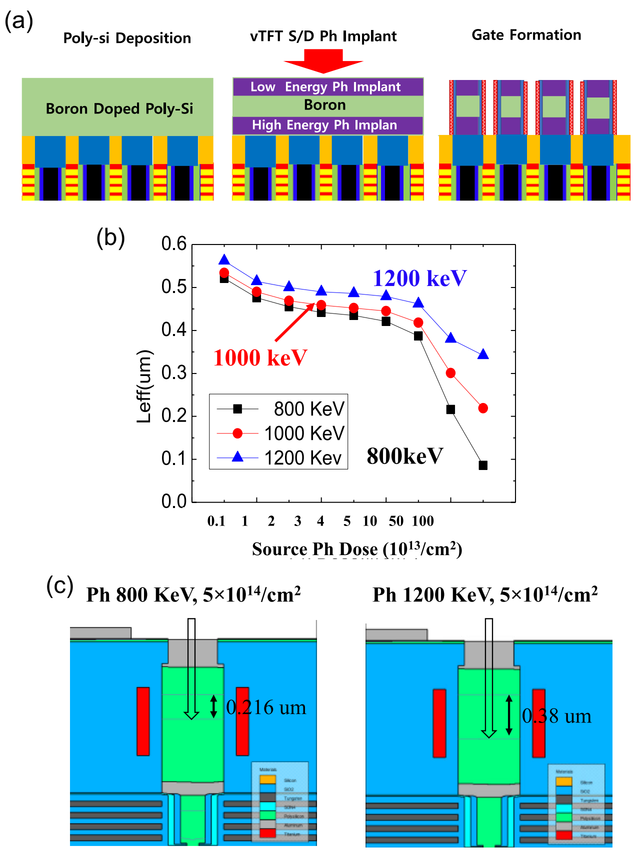
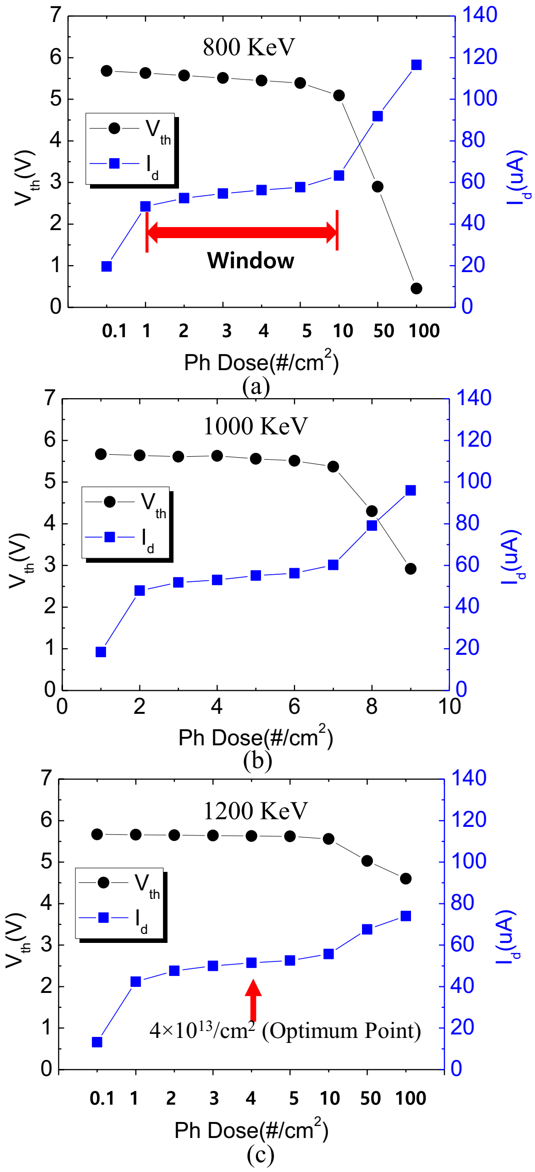


Figure 7
V_{th} and I_d characteristics depending on Ph implant dose between (a) 800 Kev, (b) 1000 KeV, and (c) 1200 KeV



3.2. vTFT transistor characteristics

Figure 6(a) describes the detailed process flow to fabricate vTFT. Figure 6(b) shows the results to optimize condition for phosphorous (Ph) implant energy and dose to form the source side of vTFT. As the Ph implant energy decreases, the results show the short channel effect as shown in Figure 6(c). Figure 7(a), (b), (c) show the process window of Ph dose for V_{th} and I_d. From this result, $4 \times 10^{13}/cm^2$ dose can be candidate as optimal value because it is located at middle point of window. In addition to vTFT characteristics depending on Ph implant energy and dose condition, the NAND flash cell characteristics should be considered as well because the cell V_{th} and I_d variation occurs by Ph penetrating to cell area as shown in Figure 8(a) and 8(b). It was explained in detail in chapter 3.3 NAND Flash cell characteristics.

Figure 8
(a) Cell V_{th} at WL2 for 4×10^{13} and 1×10^{14} Ph dose depending on Ph implant energy to fabricate vTFT and (b) I_d depending on cell V_{th} at WL = 2 for 4×10^{13} and 1×10^{14} Ph dose at Ph implant energy = 1000 KeV to fabricate vTFT

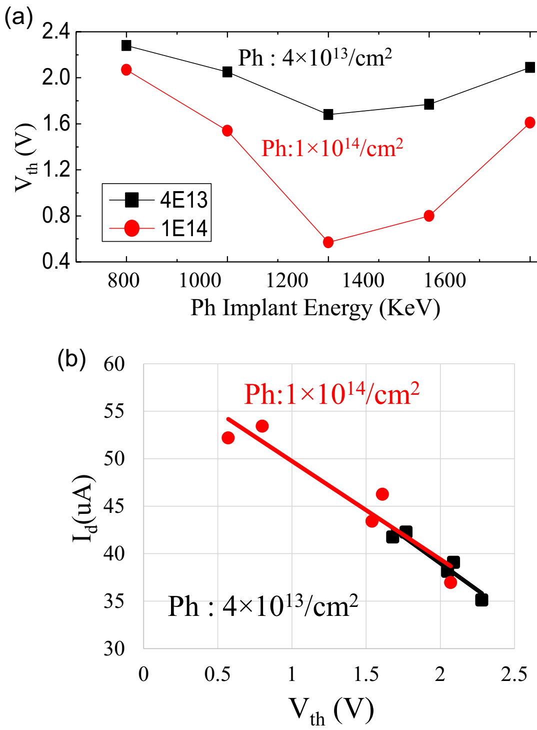


Figure 9
(a) I_d-V_g curve at WL2 depending on Ph implant energy for 800 KeV, 1000 KeV, and 1200 KeV. Channel Length depending on implant energy: (b) 800 KeV and (c) 1200 KeV

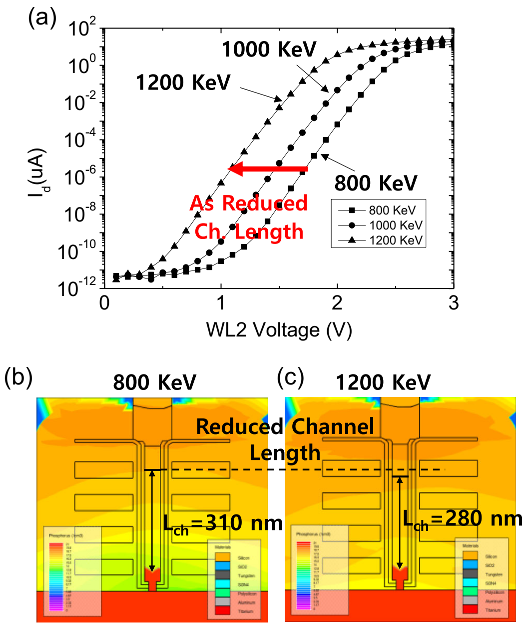


Figure 10
(a) I_d-V_g curve at WL2 depending on Ph implant energy for 1200 KeV, 1400 KeV, and 1600 KeV. Channel length depending on implant energy: (b) 1200 KeV and (c) 1600 KeV

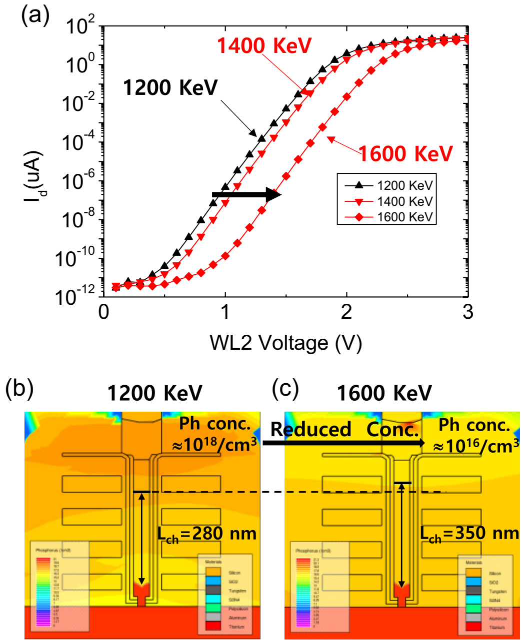


Figure 11
(a) Initial I_d-V_g depending on boron implant dose for cell channel. (b) Change of channel length depending on channel boron doping and inset shows the channel length in NAND flash cell

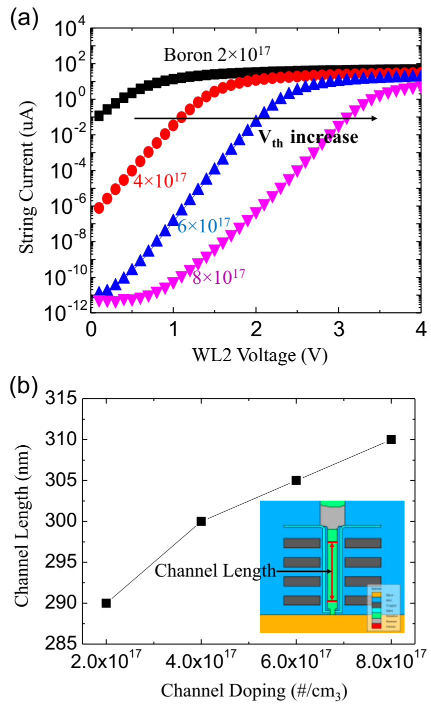
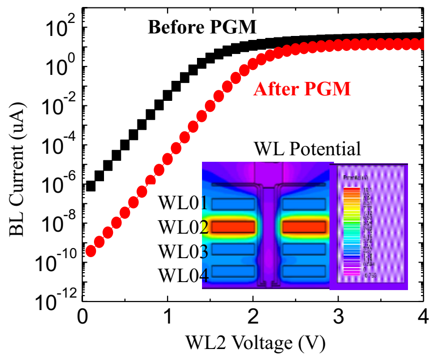


Figure 12
Program characteristics of cell at $V_{pgm} = 10V$ at WL = 2. Inset shows the WL potential at the program state



3.3. NAND flash cell characteristics

The high energy condition causes cell V_{th} to be larger variation that can be explained as two area. The high Ph implant energy between 800 and 1200 KeV makes the channel length reduced in Figure 9(a) because the main peak is formed at deeper location as shown in Figure 9(b) and (c). As Ph implant energy increases between 1200 and 1600 KeV, V_{th} becomes higher by increased channel length as shown in Figure 10(a). It is because that the main Ph peak deeply penetrates into inside NAND cell. It means the main Ph peak has passed the drain area as shown in Figure 10(b) and (c). Based on the result from Figures 7 and 8, Ph $4 \times 10^{13}/cm^2$ dose and 1000~1200 KeV energy can be proposed as the optimized conditions. Figure 11(a) shows the measured I_d-V_g and change of channel length depending on channel doping for NAND cell fabricated with optimized vTFT implant condition ($4 \times 10^{13}/cm^2$ dose and 1000 KeV energy). In Figure 11(b), the short channel effect is observed as the boron doping is lower in NAND cell channel. Additionally, it was confirmed that the program of WL02 in NAND cells is operated normally as shown in Figure 12.

4. Conclusion

Recently, a few different architectures have been proposed to overcome the issue of peripherals taking up too large an area and too high a portion of the total die size. One of them is the peripheral circuit (CMOS) can be under array (CUA) and another is to build the peripheral circuits on a different CMOS wafer and then bond the memory wafer with the CMOS wafer using wafer-to wafer micro bonding, termed as CMOS bonded array (CBA). Although the two architectures have many advantages for NAND cell, they still are suffering from the degradation of read performance due increased BL RC delay. As 3D NAND stack recently increases by 232 layers, it should be more challenging such as the degradation of RC delay due to higher stack height. Accordingly, 3D NAND flash is severely suffering from the degradation of read performance due to RC delay of bit line by higher stack height. In this paper, the COA structure using NC-vTFT was proposed to reduce the length of bit line for the first time. The COA structure consists of the SOI transistor, vTFT transistor, and 3D NAND cell with 4 layers. It was successfully fabricated using proposed process flow and the best Ion implantation conditions with Athena process simulation of Silvaco. The best process conditions were found out through the various process split conditions because the thickness of each layer gives the impact on the doping profile to operate the transistor and NAND flash cells. As a result, the optimized process condition for Ion implantation ($4 \times 10^{13}/cm^2$ dose and 1000 KeV energy) to operate the transistors and 3D NAND flash cells was secured. Also, it was finally confirmed that Program and Read for 3D NAND flash cell was normally operated.

Ethical Statement

This study does not contain any studies with human or animal subjects performed by any of the authors.

Conflicts of Interest

The authors declare that they have no conflicts of interest to this work.

Data Availability Statement

Data are available on request from the corresponding author upon reasonable request.

Author Contribution Statement

Hyowon Kang: Conceptualization, Formal analysis, Investigation, Writing – original draft, Writing – review & editing, Visualization. **Daewoong Kang:** Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation, Resources, Data curation, Supervision, Project administration.

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